AO4801/MC4801

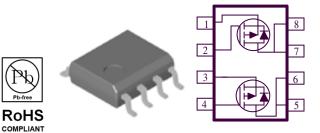
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P-Channel 20-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low r_{DS(on)} provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe SOIC-8 saves board space
- Fast switching speed
- High performance trench technology

PRODUCT SUMMARY				
V _{DS} (V)	$r_{\mathrm{DS(on)}} m(\Omega)$	I _D (A)		
	$52 @ V_{GS} = -4.5V$	-4.9		
-20	89 @ $V_{GS} = -2.5V$	-4.0		
	124 @ Vgs = -1.8V	-3.6		



ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C UNLESS OTHERWISE NOTED)						
Parameter		Symbol	Maximum	Units		
Drain-Source Voltage		V _{DS}	-20	V		
Gate-Source Voltage		V _{GS}	±12	v		
	$T_A=25^{\circ}C$	т	-5.2			
Continuous Drain Current ^a	$T_{A}=25^{\circ}C$ $T_{A}=70^{\circ}C$	ID	-4.1	А		
Pulsed Drain Current ^b		I _{DM}	±50			
Continuous Source Current (Diode Conduction) ^a		Is	-2.1	А		
	$T_A=25^{\circ}C$	D_	2.1	W		
Power Dissipation ^a	$T_{A}=25^{\circ}C$ $T_{A}=70^{\circ}C$	PD	1.3	vv		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to 150	°C		

HALOGEN

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Maximum	Units	
Maximum Junction-to-Case ^a	t <= 5 sec	$R_{\theta JC}$	40	°C/W	
Maximum Junction-to-Ambient ^a	t <= 5 sec	$R_{\theta JA}$	60	°C/W	

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Notes

a. Surface Mounted on 1" x 1" FR4 Board.

b. Pulse width limited by maximum junction temperature

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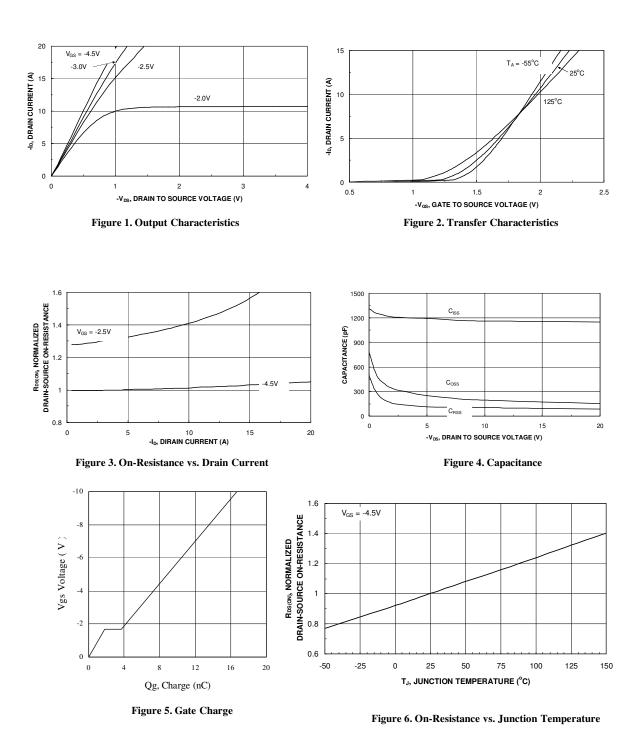
		UNLESS OTHERWISE NOTED)		T			
Parameter	Symbol	Test Conditions	Limits		T	Unit	
	-		Min	Тур	Max		
Static							
Gate-Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = -250 \text{ uA}$	-0.7				
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 12 V$			±100	nA	
Zana Cata Valtaga Drain Current	т	$V_{DS} = -16 \text{ V}, V_{GS} = 0 \text{ V}$			-1	11.4	
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = -16 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55^{\circ}\text{C}$			-5	uA	
On-State Drain Current ^A	I _{D(on)}	$V_{DS} = -4.5 \text{ V}, V_{GS} = -10 \text{ V}$	-20			Α	
		$V_{GS} = -4.5 \text{ V}, I_D = -4.9 \text{ A}$			52		
Drain-Source On-Resistance ^A	r _{DS(on)}	$V_{GS} = -2.5 \text{ V}, I_D = -4.0 \text{ A}$			89	mΩ	
		$V_{GS} = -1.8 \text{ V}, I_D = -3.6 \text{ A}$			124		
Forward Tranconductance ^A	g _{fs}	$V_{DS} = -15 \text{ V}, I_D = -4.9 \text{ A}$		20		S	
Diode Forward Voltage	V _{SD}	$I_{S} = 2.5 \text{ A}, V_{GS} = 0 \text{ V}$		-0.6		V	
Dynamic ^b							
Total Gate Charge	Qg	$V_{DS} = -10 \text{ V}, V_{GS} = -4.5 \text{ V},$		16.7		nC	
Gate-Source Charge	Q_{gs}	$v_{\rm DS} = -10$ v, $v_{\rm GS} = -4.5$ v, $I_{\rm D} = -4.9$ A		1.8			
Gate-Drain Charge	Q _{gd}	$I_{\rm D} = -4.9 \ {\rm A}$		1.9			
Turn-On Delay Time	t _{d(on)}			7			
Rise Time	t _r	V_{DD} = -10 V, R_L = 6 Ω , ID = -1 A,		13		nS	
Turn-Off Delay Time	t _{d(off)}	VGEN = -4.5 V		14			
Fall-Time	t _f			9			

Notes

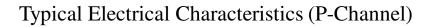
- a. Pulse test: $PW \le 300$ us duty cycle $\le 2\%$.
- b. Guaranteed by design, not subject to production testing.

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Typical Electrical Characteristics (P-Channel)



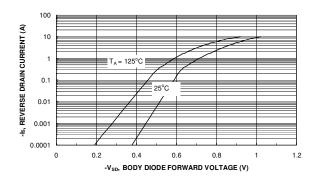


Figure 7. Source-Drain Diode Forward Voltage

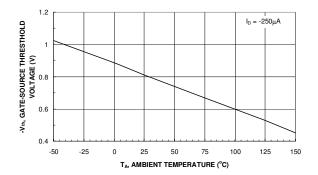


Figure 9. Vth Gate to Source Voltage Vs Temperature

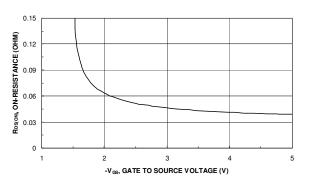


Figure 8. On-Resistance with Gate to Source Voltage

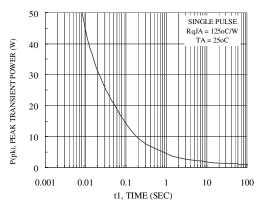
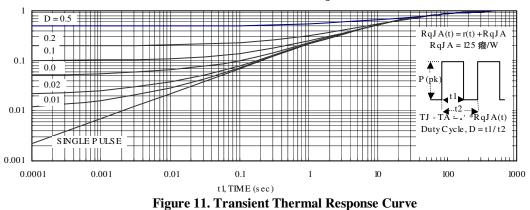


Figure 10. Single Pulse Maximum Power Dissipation



Normalized Thermal Transient Junction to Ambient

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